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EXAMINER	
STOYNOV, STEFAN	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 01/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,366	BURNS ET AL.	
	Examiner	Art Unit	
	Stefan Stoynov	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-16* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Drawings

The drawings are objected to because in Figure 1, the labels used for designating different CPU utilization levels are unreadable. In addition, in Figure 2 the Attorney Docket Number appears to be part of the drawing. In Figure 3, the 4-5us is not a valid time value designator, 4-5 μs is suggested.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities:

In the "Detailed Description" section, paragraph 0016, line 4 includes a time reference of 4-5 us, which is an invalid time value designator – 4-5 μs is suggested.

Appropriate correction is required.

Claim Objections

Claim 13 is objected to because of the following informalities:

On line 7, a plurality of processors is stated (i.e. "processors") whereas the claim refers to a single processor.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 13 rejected under 35 U.S.C. 102(e) as being anticipated by Menezes et al., US Patent No. 6,845,456.

Re claim 13, Menezes discloses a method for supervising power consumption of a processor comprising:

setting an operating point of a frequency and a voltage for the processor (column 10, lines 42-54);

operating the processor in a first power state (column 5, lines 28-30, FIG. 3, P1);

monitoring an activity level of the processor (column 3, lines 30-34, lines 48-56, column 4, lines 49-50, FIG. 2, 201, column 5, lines 2-5, column 6, lines 34-41);

transitioning the processor to a second power state when the processor's activity has increased (column 4, lines 52-60, FIG. 2, 203, 205, column 5, lines 30-36, lines 52-55), wherein

the processor operating in the second power state consumes more power than when the processor operates in the first power state (column 5, lines 28-36, lines 52-55, column 4, lines 52-60, column 1, lines 25-27).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-3, 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Menezes et al., US Patent No. 6,845,456 in view of Rundel, US Patent No. 5,914,681.

Re claim 1, Menezes discloses a method for power management of a processor comprising:

monitoring a processor utilization (column 3, lines 30-34, lines 48-56, column 4, lines 49-50, FIG. 2, 201, column 5, lines 2-5, column 6, lines 34-35);

switching from a first power state to a second power state of the processor based at least in part on the processor utilization (column 4, lines 52-60, FIG. 2, 203, 205, column 5, lines 30-36, lines 52-55); and

switching from a first frequency for the first power state to a second frequency for the second power state (column 4, lines 52-60, column 5, lines 30-36, column 10, lines 42-44, column 11, lines 57-59).

Re claim 7, Menezes discloses all claim limitations as per claim 1. In addition, Menezes discloses monitoring a processor utilization with a digital sensor (column 6, lines 35-41, lines 45-59).

Menezes fails to disclose switching from a first power state to a second power state within a single clock cycle.

Rundel teaches a fast "wakeup" of a control circuit having a powerdown feature (column 2, lines 17-19) for use in digital circuitry such as analog-to-digital converters (column 1, lines 5-9). Rundel further teaches the control circuit providing a fast wakeup operation that requires only one half of the clock cycle (column 7, lines 22-23, lines 58-60). In Rundel, the fast "wakeup" circuit and method allow for immediately beginning the analog-to-digital conversion after a very short wakeup period (column 7, lines 58-60). Thus, the digital circuit can operate at very high rate with reduced overall power dissipation (column 2, lines 1-13).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the fast "wakeup" circuit and method controlling the switchover from powerdown mode, as suggested by Rundel with the method disclosed by Menezes in order to implement. switching from a first power state to a second power state within a single clock cycle. One of

ordinary skill in the art would be motivated to do so in order to increase the processor's operational rate while reducing the overall power dissipation.

Re claims 2 and 8, Menezes further discloses the method wherein the first power state consumes less power than the second power state (column 5, lines 28-36, lines 52-55, column 4, lines 52-60, column 1, lines 25-27).

Re claims 3 and 9, Menezes further discloses the method wherein switching from the first power state to the second power state is based on a higher processor utilization (column 4, lines 52-60, FIG. 2, 203, 205, column 5, lines 30-36, lines 52-55).

Claims 4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Menezes et al., US Patent No. 6,845,456 in view of Rundel, US Patent No. 5,914,681, and further in view of Hattori, US Patent No. 6,281,727.

Re claims 4 and 10, Menezes and Rundel disclose the method of switching from a first frequency for the first power state to a second frequency for the second power state within a single clock cycle as per claims 1 and 7.

Menezes and Rundel fail to discloses receiving a timing waveform from a dual phase locked loop circuit.

Hattori teaches an improvement in finely-tuned PLLs (column 1, lines 6-7, column 2, lines 15-16) for generation of a clock implemented by two PLL loops (i.e. dual phase locked loop) (column 2, lines 17-28, column 5, lines 15-17) where the finely-tuned frequency is obtained without requiring any change to the reference frequency (column 5, lines 30-36). In addition, Hattori further teaches integration the dual-PLL clock generator with large-scale integration systems such as microprocessors (column 5, lines 36-40). Thus the desired microprocessor

clock frequency may be an abstracts frequency completely unrelated to the reference frequency, and thus improved design flexibility is achieved (column 1, lines 52-56, lines 65-67).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the dual phase PLL clock generator integrated with microprocessors, as suggested by Hattori, with the method disclosed by Menezes and Rundel in order to implement receiving a timing waveform from a dual phase locked loop circuit. One of ordinary skill in the art would be motivated to do so in order to provide a finely-tuned processor's clock signal and improved design flexibility.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oh, US Patent Appl. Pub. No. 2002/0073351.

Re claim 5, Oh discloses a method for supporting at least a first and second power state comprising:

generating a first Phase Locked Loop (PLL) clock for a first power state (paragraph 0025, lines 1-6);

generating a second Phase Locked Loop clock for a second power state (paragraph 0025, lines 7-8); and

adjusting a frequency of a processor based at least in part on the first or second power state (paragraph 0042, lines 1-6).

Oh does not specifically state adjusting a voltage of a processor based at least in part on the first or second power state. It is well known in the art that upon detection of different power states (e.g. transitioning from a low to high power state and vice versa), the processor's voltage is increased or decreased accordingly. Thus, the processor operates with the proper voltage after transitioning to the new power state, and thus the power consumption is optimized. The

examiner takes an Official Notice for adjusting a voltage of a processor based at least in part on the first or second power state. Accordingly, It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to adjust a voltage of a processor based at least in part on the first or second power state with the method discloses by Oh. One of ordinary skill in the art would be motivated to do so in order to optimize the processor's power consumption.

Claims 11, 12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Menezes et al., US Patent No. 6,845,456 in view of Oh, US Patent Appl. Pub. No. 2002/0073351.

Re claim 11, Menezes discloses a method for supervising power consumption of a processor comprising:

setting an operating point of a frequency and a voltage for the processor (column 10, lines 42-54);

monitoring an activity level of the processor (column 3, lines 30-34, lines 48-56, column 4, lines 49-50, FIG. 2, 201, column 5, lines 2-5, column 6, lines 34-35);

adjusting a frequency based on the activity level of the processor (column 4, lines 52-60, column 10, lines 42-44, column 11, lines 57-59).

Menezes fails to disclose adjusting the frequency of either a first or a second Phase Locked Loop clock.

Oh teaches a first or a second Phase Locked Loop (PLL) circuits providing adjustable clock frequencies according to the power supplying mode (paragraph 0025, lines 1-8, paragraph 0026, lines 1-7, FIG. 2). In Oh, the clock adjustment (implemented with separate PLLs) allows for lowering the frequency clocks in battery mode than in AC mode for the corresponding

devices (paragraph 0040, lines 1-3). Thus the power consumption is reduced (paragraph 0040, lines 3-4).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the method of adjusting the clock frequencies implemented by a first or a second PLL circuits, as suggested by Oh with the method disclosed by Menezes in order to implement adjusting the frequency of either a first or a second Phase Locked Loop clock. One of ordinary skill in the art would be motivated to do so in order to reduce the power consumption.

Re claim 12, Oh further teaches the method further comprising gating at least one clock to the processor to control power delivery of a functional unit of the processor (paragraph 0025, lines 1-8).

Re claim 14, Menezes discloses all claim limitations as per claim 13.

Menezes fails to disclose the method further comprising gating at least one clock to the processor to control power delivery of a functional unit of the processor.

Oh teaches a Phase Locked Loop (PLL) circuit providing adjustable clock frequencies to a CPU according to the power supplying mode (paragraph 0025, lines 1-8, FIG. 2) (i.e. the PLL circuit gating the clock provided to the CPU). In Oh, the clock adjustment (implemented with separate PLLs) allows for lowering the frequency clocks in battery mode than in AC mode for the corresponding devices (paragraph 0040, lines 1-3). Thus the power consumption is reduced (paragraph 0040, lines 3-4).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the PLL gating the clock provided to the CPU according to the power supplying mode, as suggested by Oh with the method disclosed by Menezes in order to implement method further comprising gating at least one clock to the processor to control power delivery of

a functional unit of the processor. One of ordinary skill in the art would be motivated to do so in order to reduce the power consumption.

Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams, US Patent No. 5,774,704 in view of Oh, US Patent Appl. Pub. No. 2002/0073351, and further in view of Rundel, US Patent No. 5,914,681.

Re claim 15, Williams discloses a system comprising:

an execution pipeline (column 4, lines 15-22, FIG. 2);

a digital throttle to estimate a power state, responsive to activity of the execution pipeline (column 2, lines 45-51, lines 54-57, column 4, lines 19-22, lines 27-31, lines 34-39).

Williams fails to disclose a logic to change a frequency of a first Phase Locked Loop clock.

Oh teaches a Phase Locked Loop (PLL) circuit providing adjustable clock frequencies to a CPU according to the power supplying mode (paragraph 0025, lines 1-8, FIG. 2). In Oh, the clock adjustment (implemented with separate PLLs) allows for lowering the frequency clocks in battery mode than in AC mode for the corresponding devices (paragraph 0040, lines 1-3). Thus the power consumption is reduced (paragraph 0040, lines 3-4).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the PLL circuit providing adjustable clock frequencies to the CPU according to the power supplying mode, as suggested by Oh with the system disclosed by Williams in order to implement a logic to change a frequency of a first Phase Locked Loop clock. One of ordinary skill in the art would be motivated to do so in order to reduce the power consumption.

Williams and Oh fail to disclose changing the frequency within a single clock cycle based on the power state.

Rundel teaches a fast "wakeup" of a control circuit having a powerdown feature (column 2, lines 17-19) for use in digital circuitry such as analog-to-digital converters (column 1, lines 5-9). Rundel further teaches the control circuit providing a fast wakeup operation that requires only one half of the clock cycle (column 7, lines 22-23, lines 58-60). In Rundel, the fast "wakeup" circuit and method allow for immediately beginning the analog-to-digital conversion after a very short wakeup period (column 7, lines 58-60). Thus, the digital circuit can operate at very high rate with reduced overall power dissipation (column 2, lines 1-13).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the fast "wakeup" circuit controlling the switchover from powerdown mode, as suggested by Rundel with the system disclosed by Williams and Oh in order to implement changing the frequency within a single clock cycle based on the power state. One of ordinary skill in the art would be motivated to do so in order to increase the processor's operational rate while reducing the overall power dissipation.

Re claim 16, Williams further discloses the system wherein the digital throttle comprises an activity monitor to provide an activity level response to activity states of units of the execution pipeline (column 4, lines 15-22, lines 27-31, lines 34-39).

Allowable Subject Matter

Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Re claim 6, the prior art fails to disclose or suggest, individual or in combination, the method as per claim 5, further comprising "changing a frequency of the first Phase Locked Loop

clock within a single clock cycle based on a processor utilization and changing a frequency of the second Phase Locked Loop clock after a completion of a PLL relock".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoynov whose telephone number is (571) 272-4236. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

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